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Research Article

Investigation on V_2O_5 Thin Films for Field Effect Transistor Applications

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V_2O_5 thin films are analyzed for the substitution of SiO_2 to reduce the leakage current in devices when SiO_2 becomes ultrathin in submicron technology. Vanadium pentoxide (V_2O_5) has a high-k dielectric constant of 25 and can be replaced as a gate oxide in the field-effect transistor. V_2O_5 is deposited using pulsed laser deposition (PLD) in the oxygen (O_2) environment at room temperature and characterized. The films surface morphology has been examined by scanning electron microscopy. The capacitance, dielectric constant, and dielectric loss are analyzed for fabricated metal oxide semiconductor (MOS) structure using Solartron SI-1260 impedance analyzer. The transfer characteristic of the fabricated device is analyzed using National Instruments NI-PXI 4110. The I_{ON}/I_{OFF} ratio of 10^6 and threshold voltage (V_{TH}) of 0.6 V is obtained.

1. Introduction

Thin film technology has a vital role in electronic industries. The active thin film transistor (TFT) is a part of thin film technology which is a composition of various thin layers to form the MOSFET. These layers can be formed by a device either over silicon or a glass substrate. The replacement of silicon dioxide (SiO_2) with other materials is becoming a great challenge in the community. Many developments have occurred with SiO_2, but still the current leakage in a device has not been controlled in the transistor. This current leakage leads a battery to drain in minutes in the gadgets and also reduces the efficiency by producing an enormous amount of heat. So, in order to solve this problem, material with high dielectric constant (k) of more than 3.9 has to be used [1]. Pulsed laser deposition techniques have been reported to fabricate V_2O_5 thin films [2–7]. The paper deals with the preparation of V_2O_5 using pulsed laser deposition, and its performance as a gate dielectric in MOSFET.V_2O_5 is reported as the best rare Earth materials in terms of good thermodynamic stability and high quality interface with silicon. Hence, these materials are studied for silicon FET.

2. Experimental

Many deposition techniques are available in the literature for coating the thin films. Pulsed laser deposition (PLD) technique is used for its uniform and stoichiometry deposition [8–12]. Nd-YAG laser at 355 nm is used to deposit a thin film onto the substrate, and the deposition is carried out in a chamber at oxygen (O_2) atmosphere [13–20]. The base pressure maintained during deposition is about 3.8×10^{-6} torr. The V_2O_5 (Sigma-Aldrich, 99.999%) target is placed in a sample holder which will rotate at a rate of 10 rotations per minute (rpm) during deposition. V_2O_5 thin films are deposited on the glass and silicon substrate in room

temperature [21–25]. The confirmation of V_2O_5 phase angle is done using XRD. The thin films' surface morphology is studied by scanning electron microscope (JEOL model JSM-6390), and amorphous nature of V_2O_5 films is found using X-ray diffractometer (Shimadzu model XRD-6000). The optical properties of the thin films were studied using ultraviolet spectroscopy (Shimadzu UV-240) and photoluminescence spectroscopy. The electrical properties were studied using an impedance analyzer (Solartron SI-1260) by varying the frequency. The transfer I–V characteristics of fabricated MOSFET were carried out with National Instrument PXI 4110.

3. Results and Discussion

V_2O_5 film (at R.T.) is deposited using PLD for gate dielectric.

V_2O_5 thin films are deposited at room temperature and 400°C using PLD, as shown in Figure 1. These deposited films are analyzed for the selection of the best film for the gate dielectric of FET.

3.1. Structural Analysis. The structural characterization, done by interpreting the XRD peak data, gives an insight about the crystallinity and phase changing behavior of the film when annealed at different temperatures. From the XRD plot, as in Figure 2, it is clearly shown that, as the temperature increases, the amorphous nature of the film is revealed. Deposition of the film is carried out at 400°C and subjected to vacuum annealing and then annealed at 400°C, wherein an increase in its crystalline nature is observed. The peak is observed at 17 (2theta value) for 400°C, and its (hkl Miller indices) values correspond to (002), and the system observed is orthorhombic in structure. The small peak is observed at 32.8 (2theta value) for the silicon substrate and verified from the JCPDS (78–0250), and its values corresponds to (111).

Grain size can be determined, with the Scherrer formula as

$$D = \frac{\lambda * 0.94}{\beta \cos \theta}, \tag{1}$$

where λ is the wavelength, θ is the Bragg angle, and β as the line broadening (Table 1).

The XRD pattern of V_2O_5 at room temperature, shown in Figure 2, reveals that the amorphous nature and the same film is annealed at 400°C and obtained at 2 θ at 17°. Also, the more amorphous nature of the thin film ensures a high-k dielectric value which marks its application in the fabrication of FET devices as gate dielectric.

The energy dispersive X-ray spectrum is shown in Figure 3. The observation of peaks further confirms the presence of vanadium dioxide in the deposited thin film.

3.2. Surface Topography Analysis. Figure 4 gives the SEM image of V_2O_5 at room temperature and illustrates a granular nature. The porosity increases the diffusion barrier

Figure 1: V_2O_5 thin film deposition using PLD.

properties and will have a high-resistance effect on the layer, which can be more suitable for the gate dielectric layer.

3.3. Film Morphology Analysis Using AFM. AFM image (Figure 5) shows the small step layer deposition at maximum peak difference as 833 nm over z-axis of the deposited film. It is observed for the 20 μm × 20 μm size of the placed sample. From the histogram graph, as shown in Figure 6, it is clearly observed that very few points are noted at higher peaks and all other points are almost uniformly deposited.

Observations carried out from the AFM characterization are given in Table 2. The root mean square roughness is about 125 nm and maximum peak is observed at 832 nm may be due to the ion implantation in the silicon substrate. The roughness average is noted as 96 nm which shows the smooth deposition obtained using PLD and is more suitable for the thin film transistor. The average height is 329 nm and proves the smooth deposition of the V_2O_5 thin film.

3.4. Capacitance, Dielectric Constant, and Dielectric Loss Analysis. Solartron SI-1260 is used for the analysis of capacitance, dielectric constant, and dielectric loss of V_2O_5 deposited at room temperature. Metal oxide semiconductor (MOS) structure is deposited over the N-Type silicon using the PLD technique, as shown in Figure 7. Gold is coated over the deposited film as terminals for electrodes. From equation (2), the capacitance of the MOS structure is calculated and plotted in Figure 8:

$$\mathbf{C} = \frac{\mathbf{k}.\boldsymbol{\varepsilon}.\mathbf{A}}{\mathbf{d}}. \tag{2}$$

From Figure 8, it is observed that the capacitance (in microfarad) of the MOS gradually decreases with the increase in the frequency; the amorphous state of the film has a good charging value till kilo Hz. This configured film can be more suitable for the low-frequency applications:

From equation (3) and (4), the obtain dielectric loss is

$$\tan \delta = \frac{\varepsilon''}{\varepsilon'}, \tag{5}$$

where t is thickness of the film, ω is angular frequency, Z' is the real part of impedance, Z'' is the imaginary part of impedance, $\varepsilon 0$ is permittivity of free space, and A is the area of the film.

The dielectric constant for the deposited film is observed high at low frequency and decreases with increase

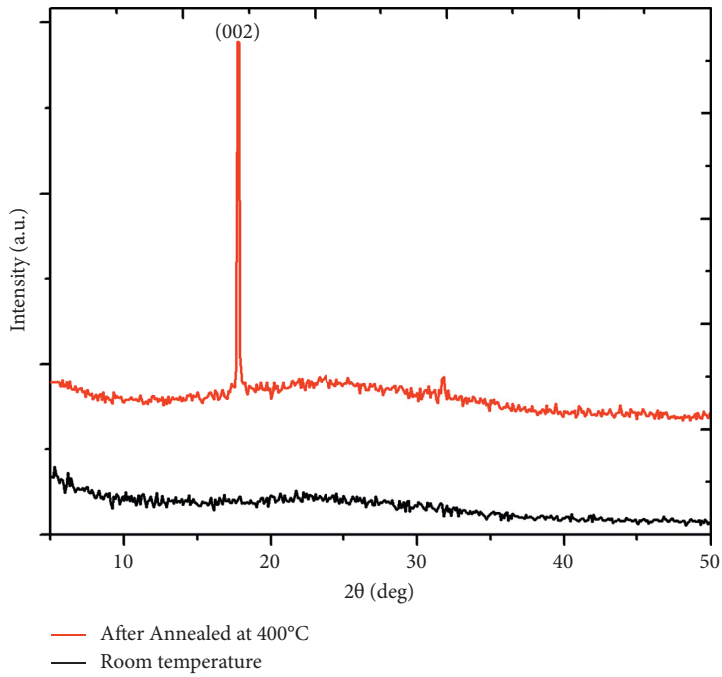

Figure 2: XRD plot of V_2O_5 at room temperature.

Table 1: The grain size of the thin films.

Sample	D (nm)
As deposited	134
400°c	185

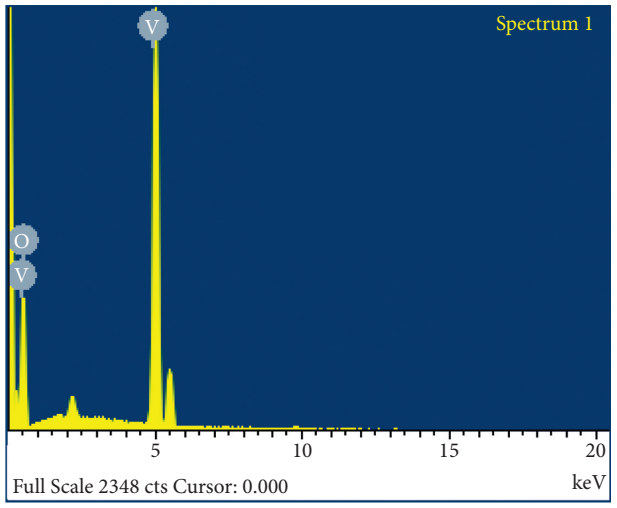

Figure 3: V_2O_5 EDAX spectra.

in frequency, as shown in Figure 9. These changes happen because of larger grain boundaries of amorphous film at the applied electric filed [23].

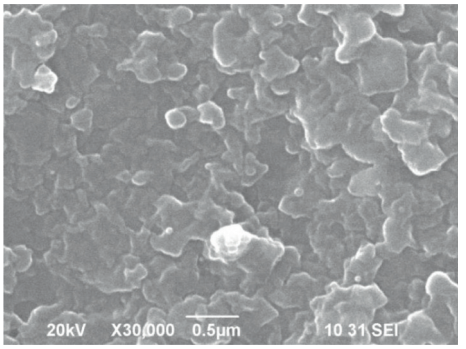

Figure 4: V_2O_5 SEM image of at room temperature.

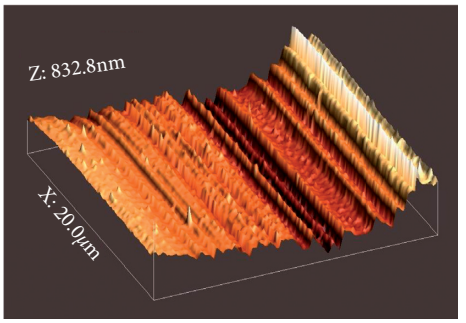

Figure 5: V_2O_5 AFM image at room temperature.

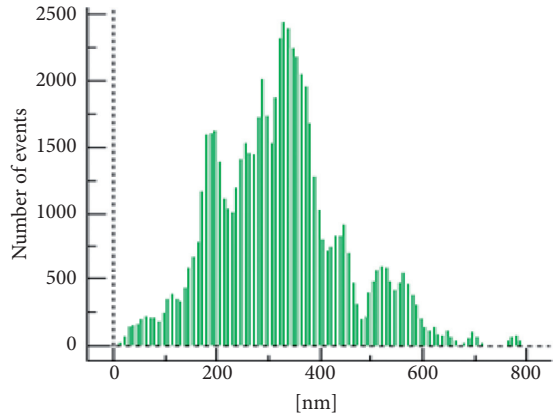

Figure 6: Histogram graph of the AFM image of V_2O_5.

Table 2: V_2O_5 parameter analysis using AFM.

RMS roughness (nm)	Maximum value (nm)	Average roughness (nm)	Average height (nm)
125	832	96	329

Figure 7: MOS structure of the V_2O_5 thin film.

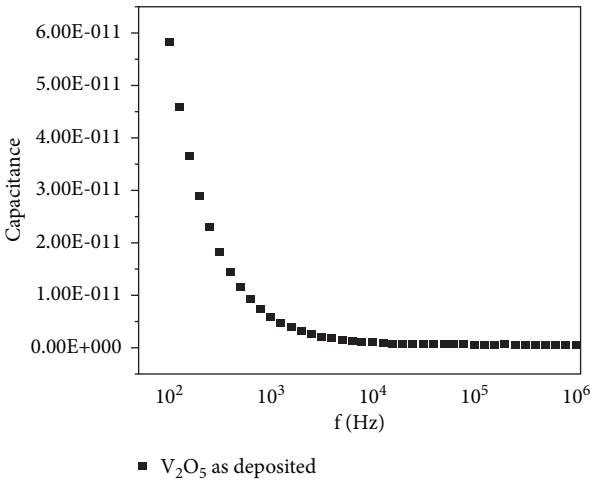

Figure 8: Capacitance vs. frequency analysis of the V_2O_5 thin film prepared at room temperature.

$$\varepsilon\prime = \frac{t}{\omega A \varepsilon 0} \cdot \frac{Z\prime\prime}{Z'^2 + Z''^2}, \tag{3}$$

$$\varepsilon\prime\prime = \frac{t}{\omega A \varepsilon 0} \cdot \frac{Z\prime}{Z'^2 + Z''^2}. \tag{4}$$

With these capacitance, dielectric constant, and dielectric loss results, the V_2O_5 thin film deposited at room temperature is more stable at low frequency and can be a better gate dielectric layer in the replacement of conventional SiO_2 in MOSFET.

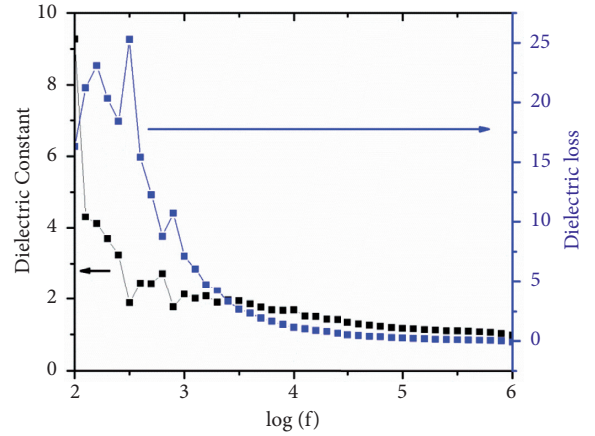

Figure 9: Dielectric constant and dielectric loss vs. log frequency of the V_2O_5 thin film prepared at room temperature.

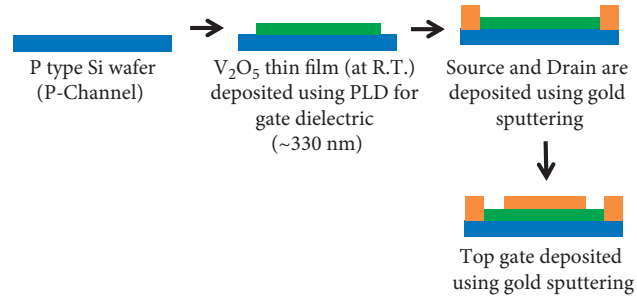

Figure 10: Fabrication steps involved in the V_2O_5 film gate dielectric-based Si-MOSFET.

4. MOSFET Fabrication

Figure 10 shows the fabrication steps of V_2O_5 thin film gate dielectric-based Si-MOSFET. In this device, P-type silicon is used as the channel and also as a base layer for the proposed

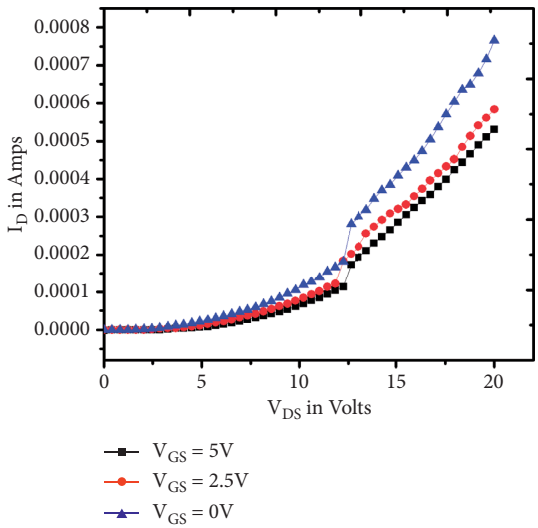

Figure 11: Output characteristics of V_2O_5 thin film gate dielectric of Si-MOSFET.

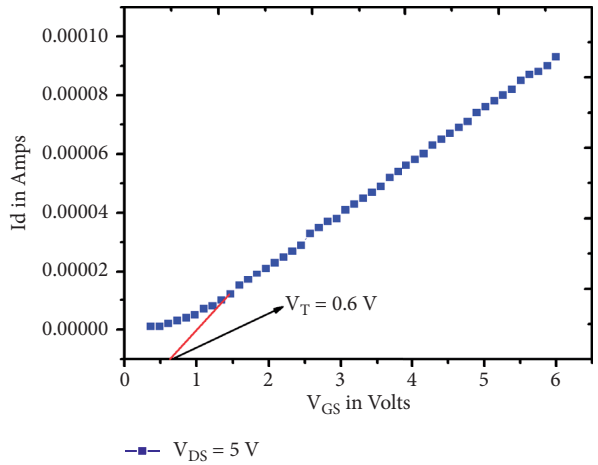

Figure 12: Transfer characteristics of V_2O_5 thin film gate dielectric of Si-MOSFET (square root of drain current vs. V_{GS}).

device. It is well cleaned and processed for the device fabrication. Inside the PLD chamber, the prepared V_2O_5 pellet is fixed as the target. With prepared stainless steel (SS) mask, the V_2O_5 thin film is deposited at 330 nm at room temperature as a gate dielectric layer. The thickness is measured using AFM. By using sputtering as the source, drain and gate are deposited with gold (Au) with the designed SS-mask.

The electrical characterization of fabricated MOSFET is carried out using National Instruments NI-4100. With the designed LabVIEW platform, the output and transfer characteristics are analyzed. Figure 11 shows the output characteristics of V_2O_5 gate dielectric-based Si-MOSFET.

In output characteristics, V_{DS} is varied between 0 and 20 Volts with various constant gate voltage (0, 2.5 V, and 5 V), and the corresponding drain current I_D is noted. Kink in the I–V characteristics is because of the sudden rise in the applied voltage (randomly set by the program), which causes this effect.

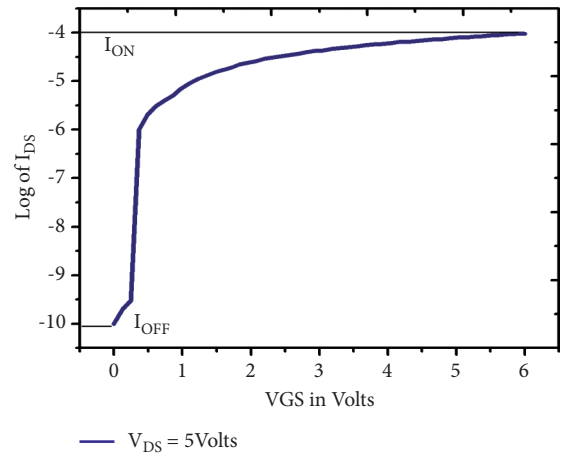

Figure 13: Transfer characteristics of V_2O_5 thin film gate dielectric of Si-MOSFET (log. of drain current vs. V_{GS}).

From Figure 12, the threshold voltage V_{TH} is found to be 0.6 V [26–29]. The I_{ON}/I_{OFF} ratio of fabricated MOSFET is calculated from the transfer characteristics results which are shown in Figure 13. The I_{ON}/I_{OFF} current ratio can be calculated by plotting the obtained drain current in the log scale; by measuring the maximum point in graph to minimum point of drain current gives the value of the I_{ON}/I_{OFF} current ratio as 10^6.

The results show that the fabricated MOSFET has less leakage current from the observed I_{ON}/I_{OFF} current and V_2O_5 thin film is more suitable for the gate dielectric of MOSFET.

5. Conclusion

The various characteristics of V_2O_5 is analyzed and reported. The replacement of SiO_2 dielectric in MOSFET is due to its large leakage current in submicron technology; the MOS structure of the V_2O_5 thin film is studied, and its capacitance, dielectric constant, and dielectric loss at low frequency are analyzed. The results revealed that the V_2O_5 thin film deposited at room temperature can be used as the gate dielectric of MOSFET. The Si-MOSFET is fabricated with V_2O_5 thin film as the gate dielectric by using PLD. It is also observed that the good I_{ON}/I_{OFF} current ratio is 10^6 and threshold voltage (V_{TH}) is 0.6 V. This I_{ON}/I_{OFF} ratio shows less leakage current with stable threshold voltage, and henceforth, the V_2O_5 thin film can be a good replacement of SiO_2 in MOSFET [30–36].

Data Availability

The data used to support the findings of this study are included within the article.

Disclosure

This study was performed as a part of the Employment of Addis Ababa Science and Technology University, Ethiopia.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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