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# Die Placement Advancement for Prevention of Silhouetted Die Occurrence on LGA Package

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***Authors' contributions***

*This work was carried out in collaboration among the authors. All authors read, reviewed and approved the final manuscript.*

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## ABSTRACT

In semiconductor packaging industry, silhouetted die defect is occasionally encountered in singulation process esp. on substrate land grid array (LGA) package with tight clearances. This paper is focused on the prevention of the silhouetted die occurrence as it would affect the assembly yield performance of the device. The silhouetted die is caused by the tight clearance of die edge to package edge, given the machine and process tolerances. Process enhancement and optimization were done through adjusting the die placement accordingly as per the defined measurement. Eventually, the occurrence of silhouetted die was successfully mitigated by formulating the appropriate die placement references.

*Keywords: BLT; die placement; LGA; silhouette.*

## 1. INTRODUCTION

Semiconductors and electronics have become an integral part of our everyday activities. As technology keeps on changing, we too must adapt to these changes. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. Meeting the customer requirements is a top priority of any

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semiconductor manufacturing company. On the other hand, failures to provide customer expectation will result to possible business failure.

New technologies like in LGA package have faced manufacturability challenges that are inherent [1-4]. Die attach process or diebonding is responsible in the picking and bonding of individually sawn silicon die from a wafer tape to the leadframe or substrate carrier. Singulation process uses a blade and it is responsible in cutting the molded leadframe into individual unit package. This paper is focused on one of the top assembly reject contributors which is the silhouetted die and this was seen after singulation process. A silhouetted die can be visualized when the silicon die is very near the edge of the package periphery but still inside the encapsulation and/or not yet exposed. On the other hand, exposed die occurs when part or parts of the die can already be seen outside the encapsulation. Fig. 1 pinpoints the signature of silhouetted die on the sideways of a singulated unit. With this issue, die attach process adjust the die placement to run this type of technology especially for Accelerometer sensor package or LGA. To guarantee its integrity during production run, die attach process and singulation process are incorporated with a multiple of criteria to prevent issues. Die attach criteria are bond line thickness (BLT), die tilting, fillet height, epoxy voids, die attach film (DAF) voids, die placement, die shear test (DST) and green peel test. Singulation criteria are dimension of X and Y axis, lead smear clearance, package off-set X and Y, solderability and visual inspection on the whole unit.

## 2. METHODS AND RESULTS

A typical assembly process flow for the LGA device is given in Fig. 2, starting from the wafer preparation or pre-assembly process then up to the singulation process. Highlighted with a green dotted line is the process where the die placement is adjusted while the highlighted in red line is the process where the silhouetted die was detected. Die attach is the process of attaching a semiconductor die on the substrate carrier, and singulation is the process of cutting into individual or singular units from the substrate strip. Important to note that assembly process flow generally varies with the technology and the product [5-8].

Silhouetted die is a top assembly reject contributor in singulation process for the device in focus, and this was seen during the lot processing on the development stage of the device. One of the challenges is to process this type of technology and to eliminate the issue

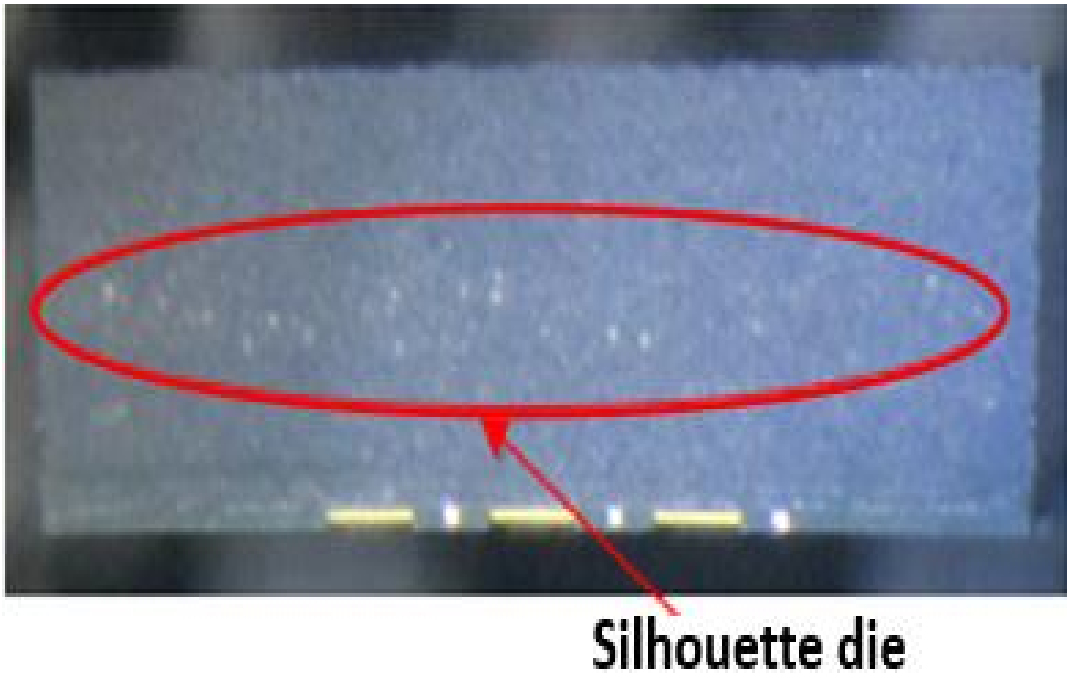



**Fig. 1. Actual reject manifestation on package side view**

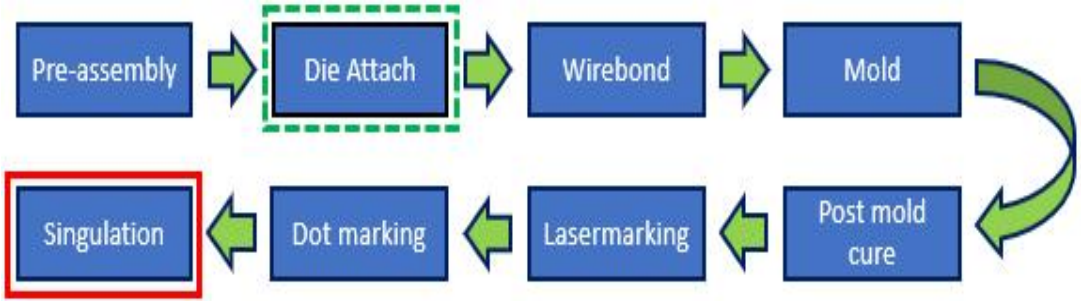



**Fig. 2. Device process flow**

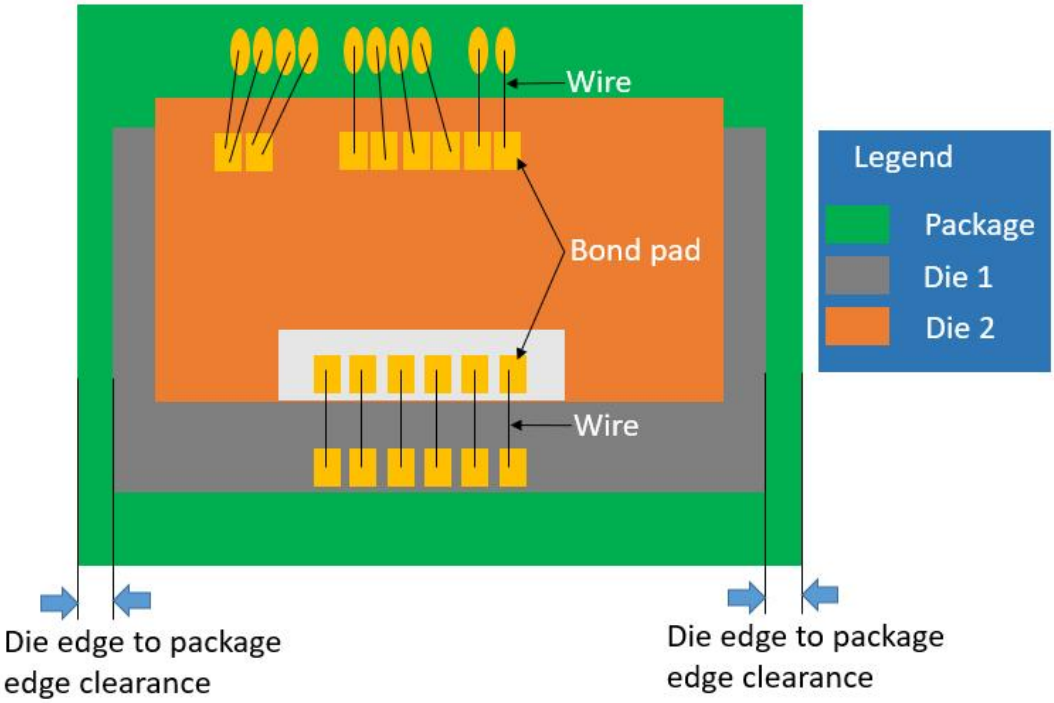


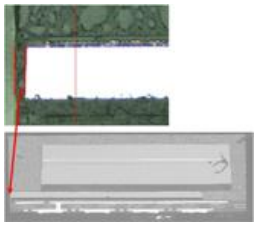
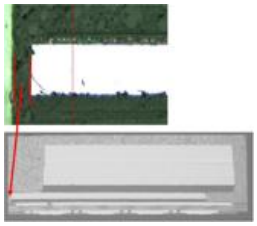
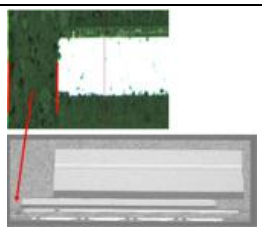

**Fig. 3. Package diagram**

encounter of silhouetted die. This issue encountered is cause by a tight die edge to package edge clearance. Fig. 3 shows the representation of the LGA package.

An improved and enhanced process solution in die attach process is widely done through moving the die placement to the right. By moving the die placement to the right, no silhouetted die occurrence is seen after implementing the improvement in die attach process. With this improvement, visual inspection on the whole package is not anymore needed, thus saving resources and time. Furthermore, faster business movement could be realized. Table 1 summarizes the die placement evaluation with scanning electron microscope (SEM) photos. The result of moving the die placement to the right form 10 microns (μm) to 20 microns has an evident of silhouetted die while moving at a higher value of 30 microns is the best solution to prevent the silhouetted die encountered at singulation process. Fig. 4 shows the reject count of silhouetted die. Note that actual numbers are intentionally not shown due to confidentiality.

Based on the die placement evaluation and the results, the optimized parameter would be to adjust the die in focus to 30 microns to the right from the original position. With this configuration, the LGA device would experience no silhouetted die occurrence.

**Table 1. Die placement evaluation summary**

| Evaluation Leg | Die Placement | SEM Photo | Remark |
|---|---|---|---|
| Leg 1 | +10 microns to the right |  | With observed silhouetted die |
| Leg 2 | +20 microns to the right |  | With observed silhouetted die |
| Leg 3 | +30 microns to the right |  | No observed silhouetted die |

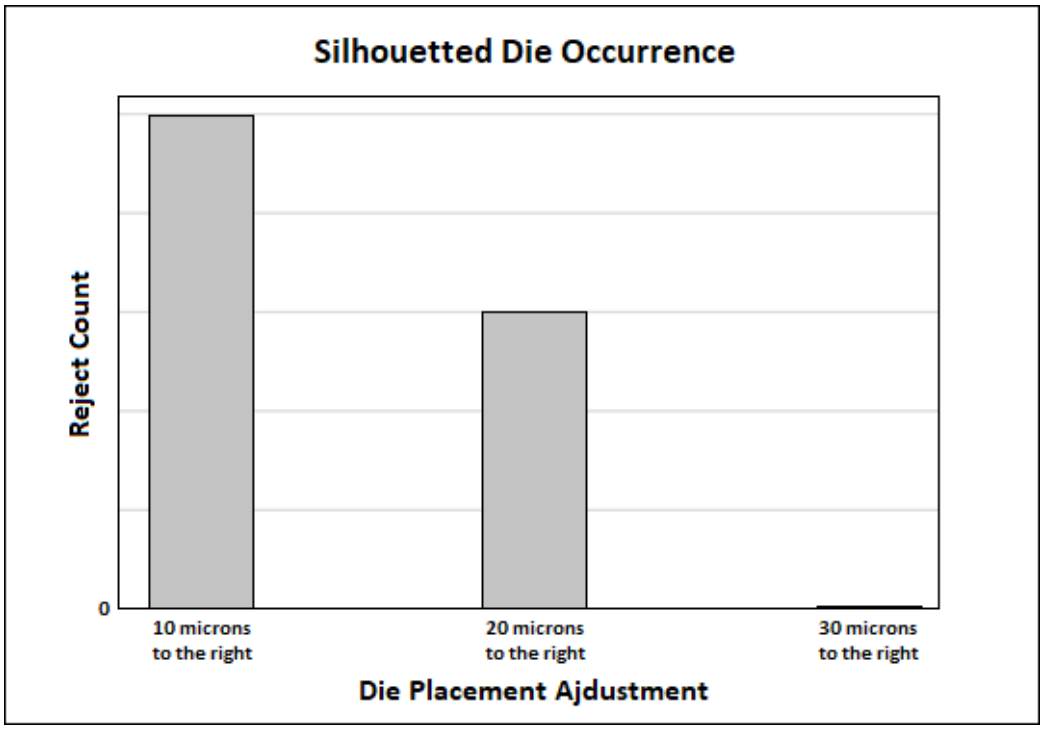



**Fig. 4. Silhouetted die reduction**

## 3. CONCLUSION AND RECOMMENDATIONS

Silhouetted die mitigation was successfully realized through comprehensive die attach process characterization and evaluation for LGA package. In this paper, it has been shown that moving the die placement of 30 microns to the right is capable to remove the occurrence of silhouetted molded strip cutting at singulation process. The die placement evaluation in this study could be used for future works on other substrate products such as ball grid array (BGA) devices with comparable configuration.

Comparison of existing works and other studies should also be included for added analysis. Worth noting is that continuous process improvement is important to sustain the high-quality performance of semiconductor products and their assembly manufacturing. Studies and learnings shared in [9-11] would help reinforce the robustness and optimization of die attach assembly process.

## DISCLAIMER

The products used for this research are commonly and predominantly used products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

## COMPETING INTERESTS

Authors have declared that no competing interests exist.

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